Clean Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(3):

'077 + 108

Sub E1

1. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

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selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer, and said depositing is

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D1 cond.

carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer; and

planarizing the conformal layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

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2. (Unchanged) A method according to Claim 1, further comprising forming a liner upon a sidewall of each said isolation trench.

3. (Unchanged) A method according to Claim 2, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

4. (Unchanged) A method according to Claim 2, wherein forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter.

5. (Unchanged) A method according to Claim 1, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

6. (Unchanged) A method according to Claim 1, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

7. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

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selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has an edge;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing with a single etch recipe the conformal layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein:

said planarizing is performed in the absence of masking the conformal layer over each said isolation trench;

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material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

said conformal layer and said spacers form said upper surface for each said isolation trench, each said upper surface being formed from said conformal layer and said spacer and being situated above said pad oxide layer; and

said first dielectric layer is in contact with at least a pair of said spacers and said pad oxide layer.

[8. ✓ (Unchanged) A method according to Claim 7, further comprising:

removing said pad oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.]

112/2nd

D3

9. ✓ (Once Amended) A method according to Claim 7, wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

112/2nd

10. (Unchanged) A method according to Claim 9, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

11. (Unchanged) A method according to Claim 7, wherein said upper surface for each said isolation trench is formed by the steps comprising:

chemical mechanical planarization, wherein said conformal layer, said spacers, and said first dielectric layer form a planar first upper surface; and

an etch that forms a second upper surface, said second upper surface being situated above said pad oxide layer.

112/2nd

12. (Unchanged) A method according to Claim 11, wherein said etch uses an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

112/2nd

13. (Unchanged) A method according to Claim 11, wherein said ratio in a range from about 1.3:1 to about 1.7:1.

14. (Thrice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon said oxide layer;

selectively removing said silicon nitride layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

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selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

poon → forming a corresponding electrically active region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, said liner being confined within each said isolation trench and extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal second silicon dioxide layer, said conformal second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second silicon dioxide layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and said silicon nitride layer; and

D4 Cond.

selectively removing said conformal second silicon dioxide layer and said spacers to form an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and being situated above said ~~pad~~ oxide layer, wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches, and wherein said selectively removing is performed in the absence of masking the conformal second silicon dioxide layer over each said isolation trench.

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15. (Unchanged) A method according to Claim 14, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

16. (Unchanged) A method according to Claim 14, wherein said liner is composed of silicon nitride.

17. (Unchanged) A method according to Claim 15, further comprising:

removing said oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

18. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

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forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and said

depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

D5 cont.

wherein planarizing the conformal third layer to form therefrom said upper surface for each said isolation trench that is co-planar to the other said upper surfaces further comprises planarizing said conformal third layer and each said spacer to form therefrom said co-planar upper surfaces, and said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

[19. (Unchanged) A method according to Claim 18, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

20. (Unchanged) A method according to Claim 18, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.]

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21. (Once Amended) A method according to Claim 18 , further comprising, prior to filling each said isolation trench with said conformal third layer, forming a liner upon a sidewall of each said isolation trench, said liner being confined within each said isolation trench and

Db cond.

extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate, and wherein said conformal third layer is composed of an electrically conductive material.

22. (Unchanged) A method according to Claim 21, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

23. (Unchanged) A method according to Claim 21, wherein forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter.

24. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

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selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and said

depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

D7 cont.

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein said upper surface for each said isolation trench is formed from said conformal third layer, said spacers, and said first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

25. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

D7 Cont.

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and said

depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

D7 Cont.

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate;

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer, in contact with a pair of said spacers; and

selectively removing said third layer, said spacers and said layer composed of polysilicon to form a portion of at least one of said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

26. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

D7 cont.

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and said

depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer by an etch using an etch recipe that etches said first dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from of about 1:1 to about 2:1 to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

D7 cond.

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

[27. (Unchanged) A method according to Claim 26, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.]

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a silicon nitride layer upon said polysilicon layer;

selectively removing said silicon nitride layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

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forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is in contact with said silicon nitride layer and said polysilicon layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding doped region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, each said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

rounding the top edges of said isolation trenches;

filling each said isolation trench with a conformal second layer, said second layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said silicon nitride layer; and

D8 cont.

planarizing said conformal second layer and each of said spacers to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and is situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

32. (Once Amended) A method according to Claim 31, wherein each said liner is a thermally grown oxide of said semiconductor substrate, and wherein said conformal second layer is composed of an electrically insulative material.

33. (Once Amended) A method according to Claim 31, wherein each said liner is composed of silicon nitride, and wherein said conformal second layer is composed of an electrically insulative material.

34. (Once Amended) A method according to Claim 31, further comprising:

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

D8 cont.

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate; and

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and

selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces.

35. (Thrice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

selectively removing said first layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a plurality of isolation trenches [having] through the exposed oxide layer at said plurality of areas, wherein electrically insulative material extend[ing]s continuously between and within said plurality of isolation trenches, each said isolation trench:

D8 cont.

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trench and extending over said spacer and over said first layer;

having a top edge and said top edge being rounded; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer, wherein said planar upper surface is

D8 cond.

formed by planarizing in the absence of masking said second layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

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36. (Unchanged) The method as defined in Claim 35, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each said isolation trench.

37. (Unchanged) The method as defined in Claim 36, wherein the doped trench bottom has a width, each said the isolation trench has a width, and the width of each said doped trench bottom is greater than the width of the respective isolation trench.

38. (Four Times Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

selectively removing said first layer to expose said oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the oxide layer at said plurality of areas, wherein electrically insulative material extends continuously between and within said plurality of isolation trenches, each said isolation trench:

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having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trench and extending over said spacer and over said first layer;

having a top edge and said top edge being rounded; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer, wherein said planar upper surface is formed by planarizing in the absence of masking said second layer over each of said isolation trenches; and

D9 cont.

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

39. (Unchanged) The method as defined in Claim 38, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of said isolation trenches.

40. (Unchanged) The method as defined in Claim 39, wherein:

the doped trench bottom has a width;

each said isolation trench has a width; and

the width of each said doped trench bottom is greater than the width of the respective isolation trench.

41. (Cancelled)

42. (Four Times Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded;

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a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of said semiconductor substrate and below said oxide layer

into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is curved;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

D10 cont.

rounding the top edges of said isolation trenches;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trenches and extending over said spacers and over said first layer; and

forming with a single etch recipe a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer; and

D10 cont.

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

43. (Four Times Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded;

D10 cont.

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench,

and wherein said first isolation trench in said second isolation structure has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

D10 cnd.

forming a conformal second layer, composed of an electrically insulative material, conformally filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trenches and extending over said spacers and over said first layer; and

planarizing the conformal second layer and said first and second spacers of said respective first and second isolation structures to form a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches, and wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches.